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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 14

Application Number: 09/418,031
Filing Date: October 14, 1999
Appellant(s): JANG ET AL.

Stephen B. Ackerman
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/3/2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The appellant's statement of the grouping of claims in the brief is correct.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,100,184	ZHAO et al	8-2000
5,968,842	HSIAO	10-1999
5,192,715	SLIWA et al	3-1993
5,759,911	CRONIN et al	6-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-7, 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al. (US 6,100,184) in view of Hsiao (US 5,968,842)

Zhao discloses a method for making a dual damascene interconnect. This method comprises the step of:

forming a substrate having a conductive region (contact region) 10 (col 4, lines 14-16)

forming over the substrate a lower etch stop layer 13 (silicon oxide) and an upper dielectric layer 14 (col 6, lines 33-65 and fig. 2) reads on forming over the substrate a first lower sub-layer and a second upper sub-layer

forming over the lower layer 13 and upper layer 14, an interlevel dielectric (ILD) layer 15 (silicon dioxide) (col 6, lines 23-25)

forming over the IDL layer a photoresist mask pattern 22 to define a subsequent via opening and trench opening over the contact region (col 7, lines 19-23 and fig. 7), utilizing a first plasma etching to etch through the ILD layer 15 and upper layer 14 to the lower layer 13 (col 7, lines 24-45 and fig. 9)

employing a second etch method to etch the lower layer 13 from the trench pattern for the interconnect (col 8, lines 2-5)

Zhao differs from the instant claimed invention as per claim 1 by using a lower layer 13 (silicon oxide) as an etch stop layer instead of a composite etch stop layer.

However, Hsiao discloses a method for reducing dishing in CMP comprises the steps of forming a composite polish stop layer/etch stop layer includes two sub-layers

32 and 34 (silicon nitride and oxynitride) (col 6, lines 43-46). That teaching reads on forming a composite etch stop layer includes two sub-layers.

Since Zhao teaches forming lower etch stop layer and upper dielectric layer on the conductive region before the etching step, one skilled in the art would have found it obvious to combine Zhao's lower etch stop layer and upper dielectric layer to form a composite etch stop layer in view of Hsiao's teaching in order to achieve higher etch selectivity with respect to the conductive region.

Regarding claim 2, fig. 9 of Zhao shows that lower layer 13 prevents the first etching method from etching the contact region.

Regarding claim 3, fig. 10 of Zhao shows that the second etching step removes the lower layer 13 without etching the contact region.

Regarding claim 4, Zhao further discloses the steps of:

forming a barrier metal layer 28 (TaN) over the substrate and filling the trench with a conductor material to complete the interconnection structure (col 8, lines 35-40)

Regarding claims 5-6, Zhao's method of making a interconnect structure on a semiconductor substrate reads on forming a microelectronics semiconductor layer on a integrated circuit microelectronic fabrication.

Regarding claim 7, Zhao discloses forming the lower layer 13 by CVD (col 6, lines 3-4)

Regarding claim 9, it is known in the art to fill contact region with tungsten

Regarding claim 10, Zhao discloses that the ILD layer 15 is formed by CVD (col 6, lines 24-26)

Regarding claim 11, Zhao discloses filling the trench with copper (col 8, lines 43-44)

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al. (US 6,100,184) in view of Hsiao (US 5,968,842) and further in view of Sliwa et al. (US 5,192,715)

Zhao as modified by Hsiao has been described above. Zhao and Hsiao differs from the instant claimed invention as per claim 8 by forming a upper dielectric layer of low k dielectric material such as polyimide instead of silicon oxynitride.

However, Sliwa teaches that dielectric layer include polyimide, silicon oxynitride (col 4, lines 1-3)

Hence, one skilled in the art would have found it obvious to substitute Zhao's upper layer of polyimide with silicon oxynitride in view of Sliwa's teaching because polyimide and silicon oxynitride are equivalent dielectric material and substitution of one for the other would have been anticipated to produce an expected result.

Claims 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al. (US 6,100,184) in view of Hsiao (US 5,968, 842) and further in view of Cronin et al. (US 5,759,911)

Zhao discloses a method for making a dual damascene interconnect. This method comprises the step of:

forming a substrate having a aluminum conductive region (contact stud) 10 (col 4, lines 14-16)

forming over the substrate a lower dielectric organic polymer layer 14 (polyimide) and a upper dielectric etch stop layer 15 (col 6, lines 10-25 and fig. 3) reads on

forming over the substrate a first lower organic polymer sub-layer and a second upper sub-layer

forming over the lower layer 14 and upper layer 15, an interlevel dielectric (ILD) layer 19 (silicon dioxide) (col 6, lines 61-65)

forming over the IDL layer a photoresist mask pattern 22 to define a subsequent via opening and trench opening over the contact region (col 7, lines 19-23 and fig. 7), utilizing a first plasma etching to etch through the ILD layer 19 and upper layer 15 to the lower polymer layer 14 (col 7, lines 25-34)

removing/stripping the photoresist mask and simultaneously etching the lower polymer layer 14 to complete the interconnection over the aluminum contact region (col 7, lines 30-45)

Zhao differs from the instant claimed invention as per claim 12 by using an upper layer 15 (silicon oxide) as an etch stop layer instead of a composite etch stop layer and using a contact region of aluminum instead of tungsten.

However, Hsiao discloses a method for reducing dishing in CMP comprises the steps of forming a composite polish stop layer includes two sub-layers (silicon nitride and oxynitride) (col 6, lines 43-46). That teaching reads on forming a composite etch stop layer includes two sub-layers.

Since Zhao teaches forming lower etch stop layer and upper dielectric layer on the conductive region before the etching step, one skilled in the art would have found it obvious to combine Zhao's lower etch stop layer and upper dielectric layer to form a

composite etch stop layer in view of Hsiao's teaching in order to achieve higher etch selectivity with respect to the conductive region.

Zhao and Hsiao differ from instant claimed invention as per claim 12 by using a contact region of aluminum instead of tungsten.

Cronin teaches that aluminum or tungsten can be used to fill contact region or stud connection in a semiconductor structure (col 10, lines 3-5)

Hence, one skilled in the art would have found it obvious to substitute Zhao and Hsiao aluminum contact stud with tungsten stud in view of Cronin's teaching because aluminum and tungsten are equivalent conductive material and substitution of one for the other would have been anticipated to produce an expected result.

Regarding claim 14, Zhao discloses forming a barrier metal layer 28 (TaN) over the substrate and filling the trench with a conductor material to complete the interconnection structure (col 8, lines 35-40)

Regarding claim 16, Zhao discloses that lower polymer layer comprises of low dielectric constant spin-on-polymer such as polyimide (col 6, lines 15-17)

Regarding claim 17, Zhao discloses that upper layer 15 (silicon dioxide) is formed by CVD (col 6, lines 24-26)

Regarding claim 19, Zhao discloses filling the trench with aluminum or copper (col 8, lines 43-44

(11) Response to Argument

In traversing the examiner rejection of claims 1 and 12, the applicants argue that Zhao (the primary reference) does not teach the method of applicant's invention

because the method employed by Zhao requires the employment of two or more additional dielectric layers than does the applicant's invention to accomplish the formation of the inlaid pattern. This argument is not found persuasive because although the examiner recognizes that Zhao's method requires two additional dielectric layers to accomplish the formation of inlaid pattern, however, the language of "a method for forming a patterned microelectronic layer comprising", as recited in claims 1 and 12, does not exclude the use of additional dielectric layers in the claimed method. Thus, the examiner asserts that Zhao's method reads on the claimed inventions as per claims 1 and 12.

The applicants further argue that the cited reference do not teach the simultaneous removal of the organic polymer sub-layer with that of the photoresist etch mask layer. The examiner disagrees because as recited in col 7, lines 31-39 of Zhao, Zhao discloses using a plasma etch to strip/remove the photoresist mask layer 22 and polyimide sub-layer 14 (claimed organic polymer sub-layer). This teaching of Zhao certainly reads on the cited reference do not teach the simultaneous removal of the organic polymer sub-layer with that of the photoresist etch mask layer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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